

FIG. 1

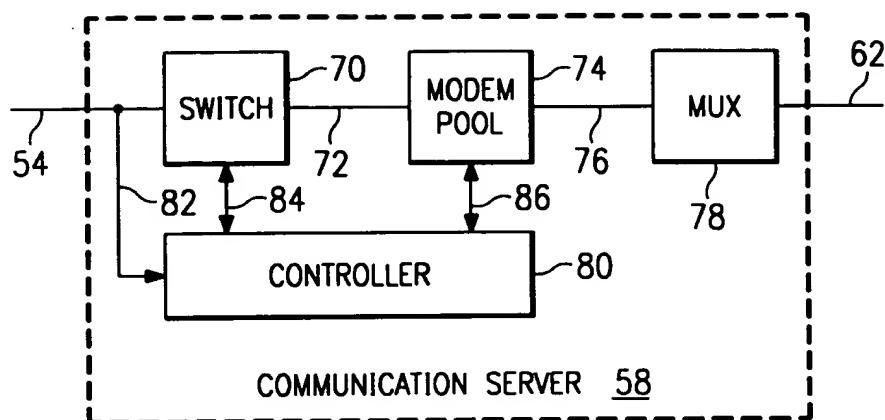


FIG. 2

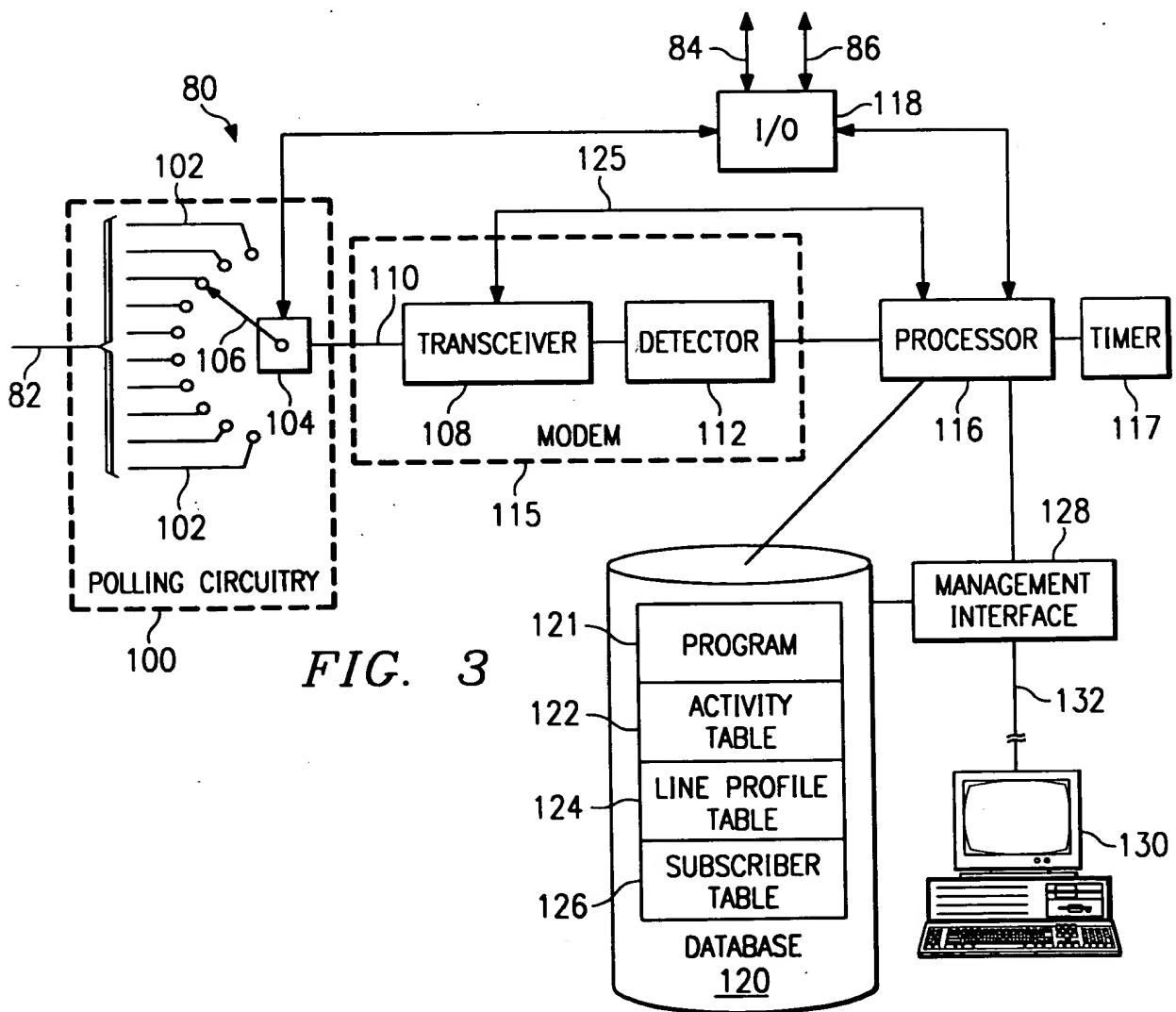
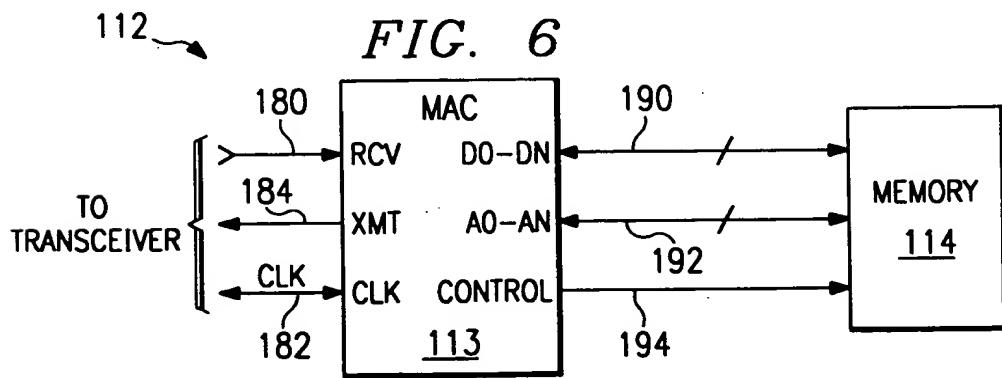
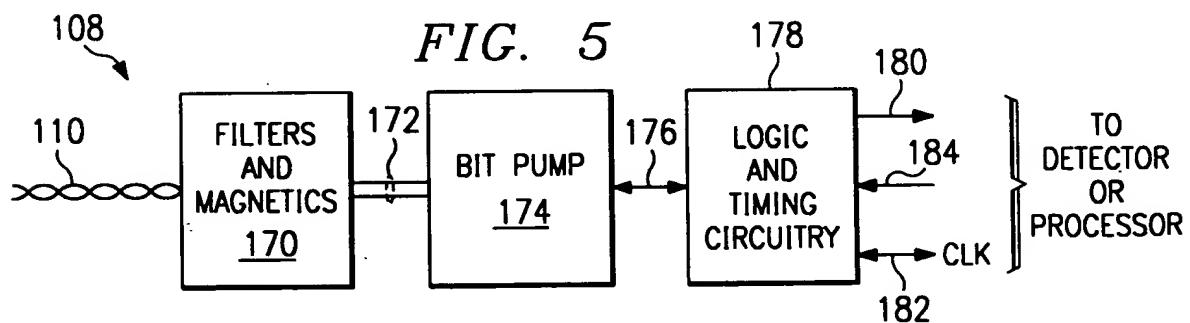
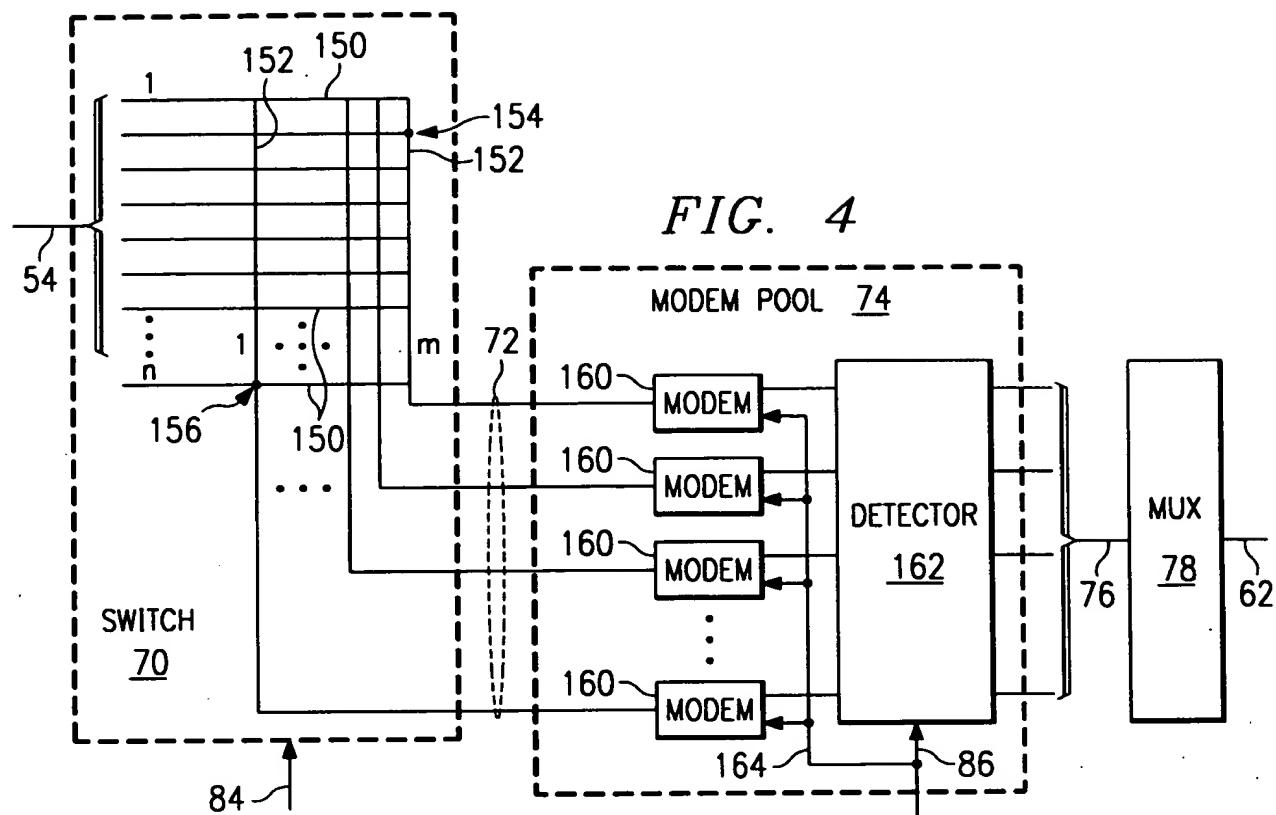


FIG. 3



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DATA LINE	STATUS	TIMEOUT	MODEM
D1	I	-	-
D2	I/D	-	M1
D3	I	-	-
D4	A	T	M3
D5	I	-	-
D6	I	-	-
D7	A/D	-	M2
D8	A	-	M4
D9	I	-	-
D10	I	-	-

FIG. 7

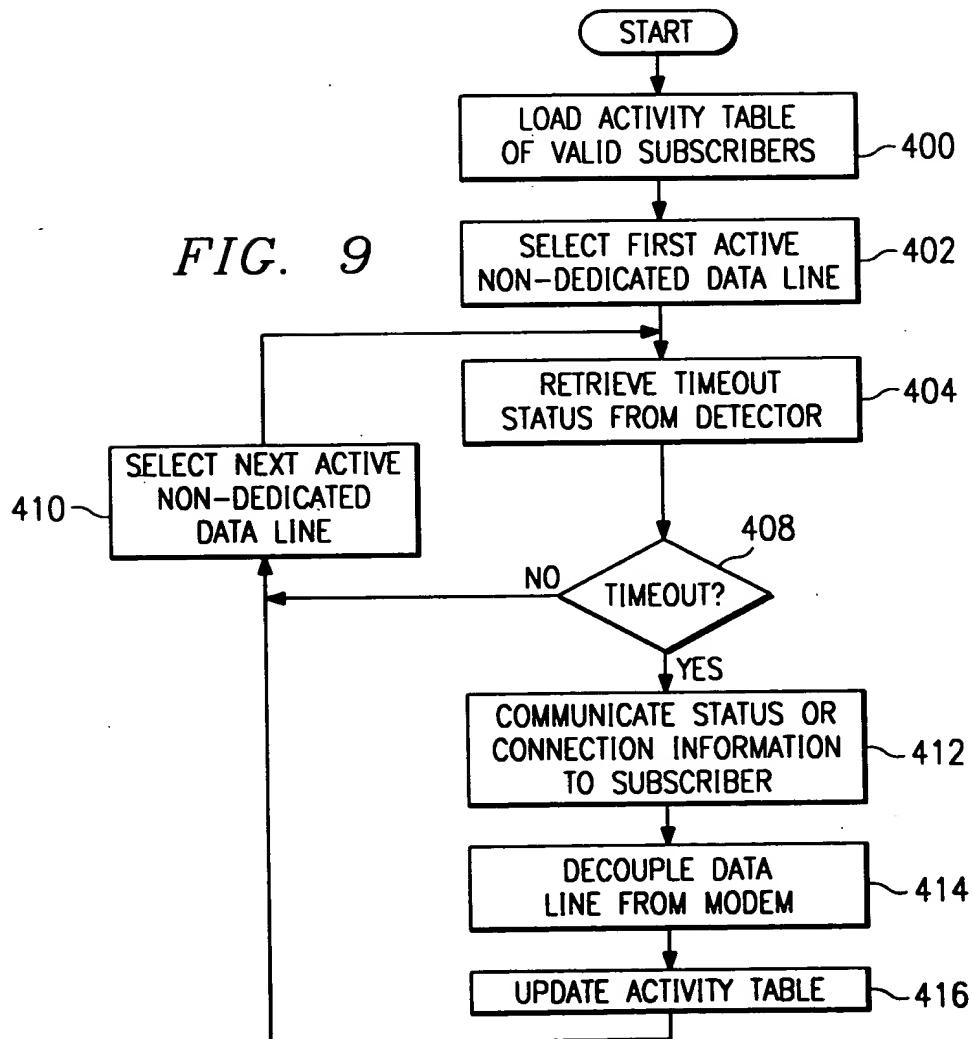
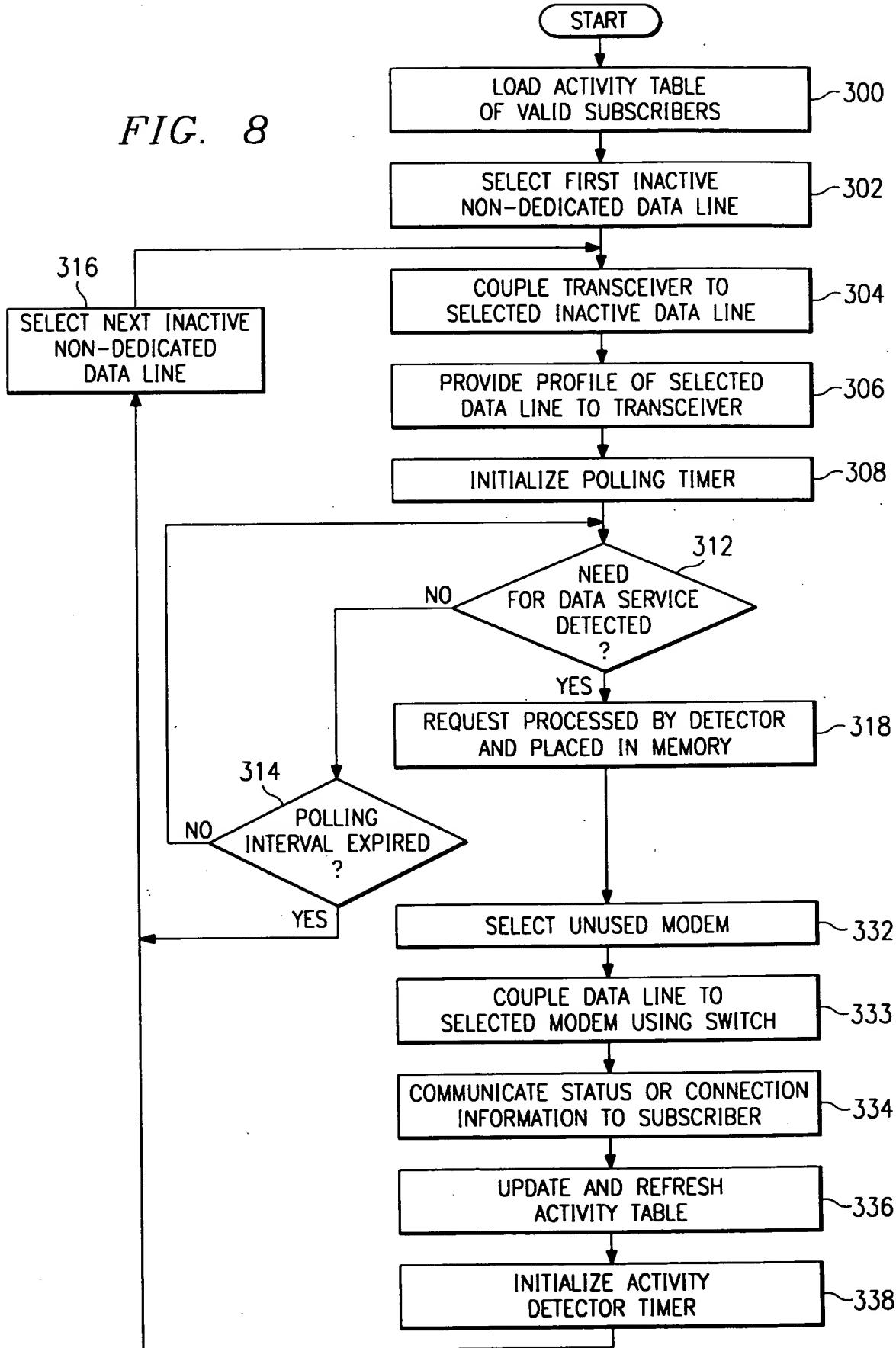


FIG. 8



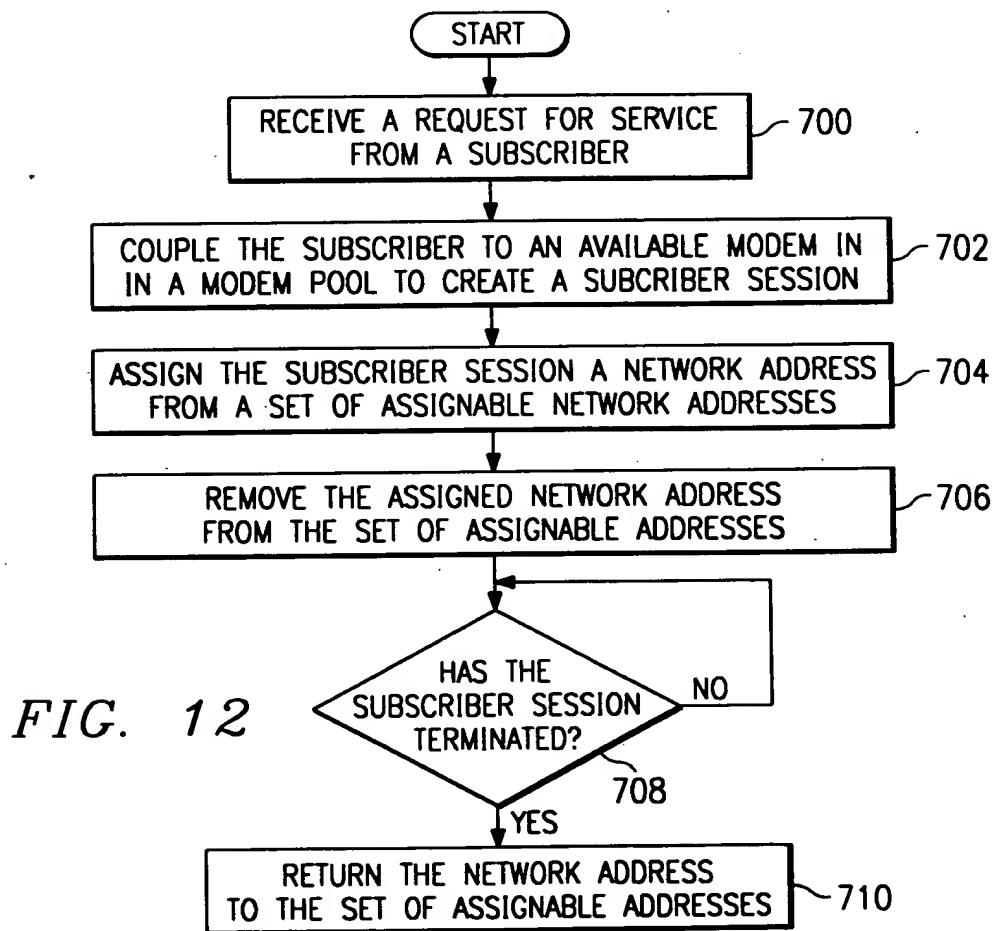
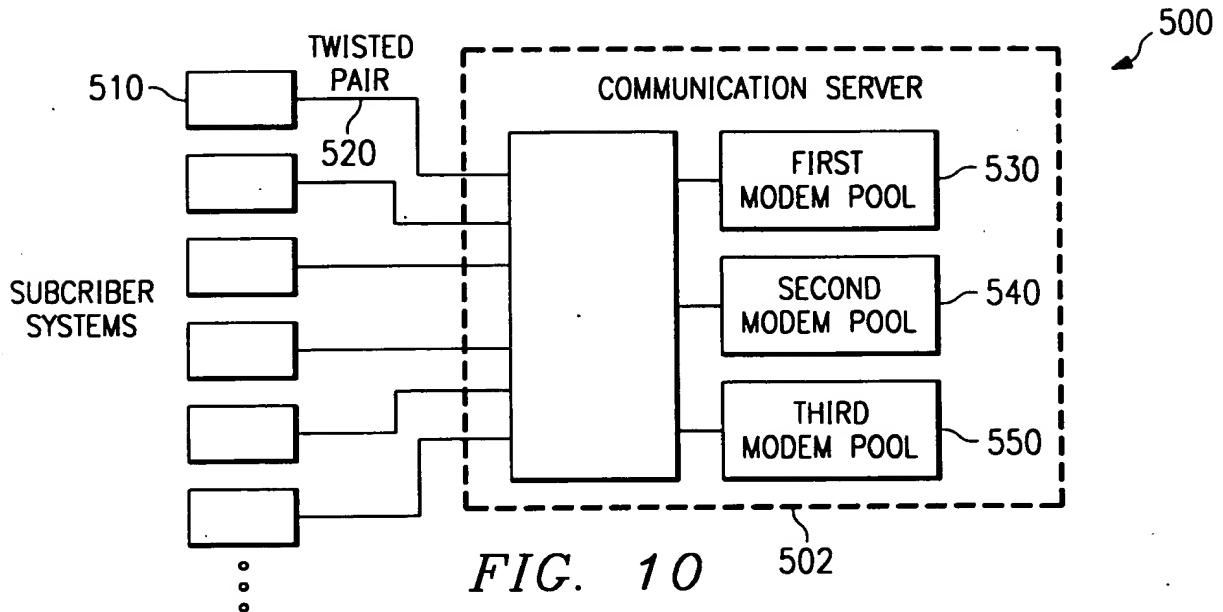


FIG. 11

